AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions and listings of claims in the application.

1. (Canceled)

2. (Currently Amended) A method for fabricating a semiconductor device comprising:

forming a conductor pattern over a semiconductor substrate;

forming over the conductor pattern a first insulation film;

forming a conductive region in the semiconductor substrate;

forming, over the semiconductor substrate with the conductor pattern, the conductive region and the conductor pattern formed, a second insulation film having etching characteristics different from those of the first insulation film and having a ~~substantially flat~~ planarized surface;

forming over the second insulation film a third insulation film having etching characteristics different from those of the second insulation film;

forming over the third insulation film a fourth insulation film having etching characteristics different from those of the third insulation film;

forming over the fourth insulation film a mask layer;

forming a hole reaching down to the conductive region in the fourth insulation film, the third insulation film and the second insulation film, forming the hole including a first step of etching the fourth insulation film, a second step of etching the third insulation film and a third step of etching the second insulation film, an etching condition at the first step being different from that at the second

step, in the third step of etching the second insulation film, the second insulation film being etched with the first insulation film as a stopper;

forming a conductive material in the hole to form a contact conducting film of the conductive material, the contact conducting film being electrically connected to the conductive region;

forming over the fourth insulation film an interconnection pattern electrically connected to the contact conducting film; and

forming a fifth insulation film over the interconnection pattern.

3. (Previously Presented) A method for fabricating the semiconductor device according to claim 2, wherein

in forming the conductor pattern, the conductor pattern is formed over a first region of the semiconductor substrate;

in forming the first insulation film, the first insulation film is selectively formed over a side wall of the conductor pattern; and

in the third step of etching the second insulation film, the second insulation film is etched to form the opening exposing in a part of a bottom thereof a second region of the semiconductor substrate, which is other than the first region, and exposing in another part of the bottom thereof the first insulation film.

4. – 18. (Canceled)

19. (Previously Presented) A method for fabricating the semiconductor device according to claim 2, wherein

in the first step of etching the fourth insulation film, the fourth insulation film is etched with the third insulation film as a stopper.

20-22. (Canceled)

23. (Previously Presented) A method for fabricating the semiconductor device according to claim 2, further comprising forming capacitors, bit lines and wiring layers to constitute a memory device.

24. (Previously Presented) A method for fabricating the semiconductor device according to claim 2, wherein the second insulation film comprises silicon oxide.

25. (Previously Presented) A method for fabricating the semiconductor device according to claim 2, wherein the third insulation film comprises silicon nitride.

26. (Previously Presented) A method for fabricating the semiconductor device according to claim 2, wherein the fourth insulation film comprises silicon oxide.

27. (Canceled)

28. (Previously Presented) A method for fabricating the semiconductor device according to claim 2, wherein

in forming the hole, an etching rate of the third insulation film when the third insulation film is etched with an etching condition at the first step of etching the fourth insulation film is lower than an etching rate of the fourth insulation film at the first step of etching the fourth insulation film and an etching rate of the third insulation film at the second step of etching the third insulation film.

29. (Currently Amended) A method for fabricating a semiconductor device comprising:

forming a conductor pattern over a semiconductor substrate;

forming over the conductor pattern a first insulation film;

forming over the semiconductor substrate with the conductor pattern and the conductor pattern formed a second insulation film having etching characteristics different from those of the first insulation film and having a ~~substantially flat~~ planarized surface;

forming over the second insulation film a third insulation film having etching characteristics different from those of the second insulation film;

forming over the third insulation film a fourth insulation film having etching characteristics different from those of the third insulation film;

forming over the fourth insulation film a mask layer;

forming a hole reaching down to the conductor pattern in the fourth insulation film, the third insulation film and the second insulation film, forming the hole including a first step of etching the fourth insulation film, a second step of etching the third insulation film and a third step of etching the second insulation film, an etching condition at the first step being different from that at the second step, in the third step of etching the second insulation film, the second insulation film being etched with the first insulation film as a stopper;

forming a conductive material in the hole to form a contact conducting film of the conductive material, the contact conducting film being electrically connected to the conductor pattern;

forming over the third insulation film an interconnection pattern electrically connected to the contact conducting film; and

forming a fifth insulation film over the interconnection pattern.

30. (Previously Presented) A method for fabricating the semiconductor device according to claim 29, wherein

in forming the conductor pattern, the conductor pattern is formed over a first region of the semiconductor substrate;

in forming the first insulation film, the first insulation film is selectively formed over a side wall of the conductor pattern; and

in the third step of etching the second insulation film, the second insulation film is etched to form the opening exposing in a part of a bottom thereof a second region of the

semiconductor substrate, which is other than the first region, and exposing in another part of the bottom thereof the first insulation film.

31. (Previously Presented) A method for fabricating the semiconductor device according to claim 29, wherein

in the first step of etching the fourth insulation film, the fourth insulation film is etched with the third insulation film as a stopper.

32. (Previously Presented) A method for fabricating the semiconductor device according to claim 29, further comprising forming capacitors, bit lines and wiring layers to constitute a memory device.

33. (Previously Presented) A method for fabricating the semiconductor device according to claim 29, wherein the second insulation film comprises silicon oxide.

34. (Previously Presented) A method for fabricating the semiconductor device according to claim 29, wherein the third insulation film comprises silicon nitride.

35. (Previously Presented) A method for fabricating the semiconductor device according to claim 29, wherein the fourth insulation film comprises silicon oxide.

36. (Previously Presented) A method for fabricating the semiconductor device according to claim 29, wherein

in forming the hole, an etching rate of the third insulation film when the third insulation film is etched with an etching condition at the first step of etching the fourth insulation film is lower than an etching rate of the fourth insulation film at the first step of etching the fourth insulation film and an etching rate of the third insulation film at the second step of etching the third insulation film.

37. (Previously Presented) A method for fabricating the semiconductor device according to claim 29, wherein

in forming the first insulation film, the first insulation film is formed so as to expose at least a part of the conductor pattern.